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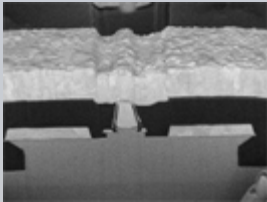
# ***High-Frequency Transistors High-Frequency ICs***

## ***Technologies & Applications***

***Mark Rodwell  
University of California, Santa Barbara***

Report Documentation Page				Form Approved OMB No. 0704-0188	
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# UCSB High-Frequency Electronics Group



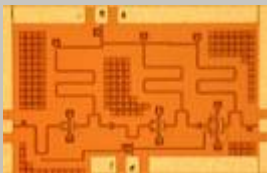
## Ultra High-Frequency III-V Transistors:

Aim for 1-2 THz cutoff frequencies  
InGaAs/InP bipolar transistors  
InGaAs/InP field-effect transistors



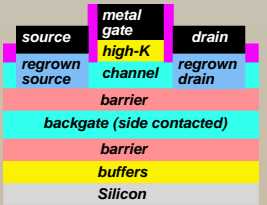
## Ultra High Frequency III-V ICs

Aim for 500+ GHz digital clock rates  
Aim for 700+ GHz amplifiers  
other advanced circuits



## mm-wave ICs in Silicon (60-90 GHz)

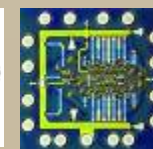
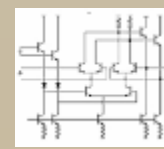
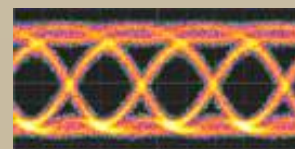
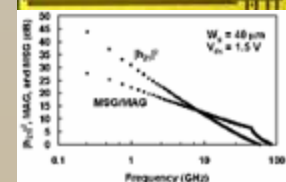
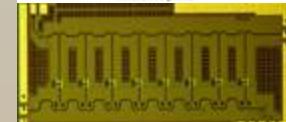
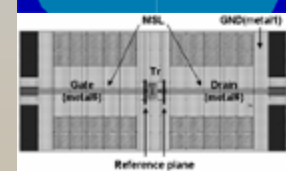
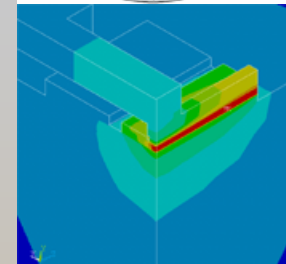
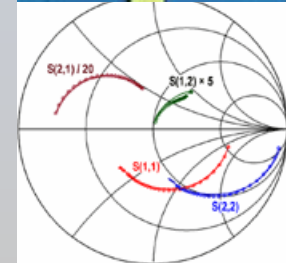
10-160 Gb/s wireless,  
mm-wave sensor networks  
monolithic arrays for radar & communications  
mm-wave MIMO



## III-V CMOS for Si VLSI

III-V channel MOSFETs for sub-22-nm scaling

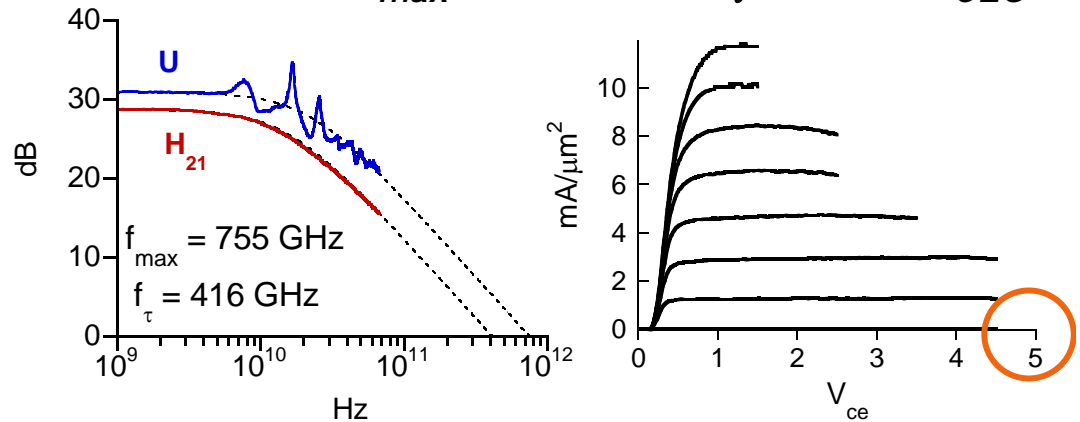
DARPA  
ONR  
SRC  
NSF



# THz Transistors are coming soon

*InP Bipolars: 250 nm generation:  $\rightarrow 750 \text{ GHz } f_{max}, 400 \text{ GHz } f_{\tau}, 5 \text{ V } BV_{CEO}$*

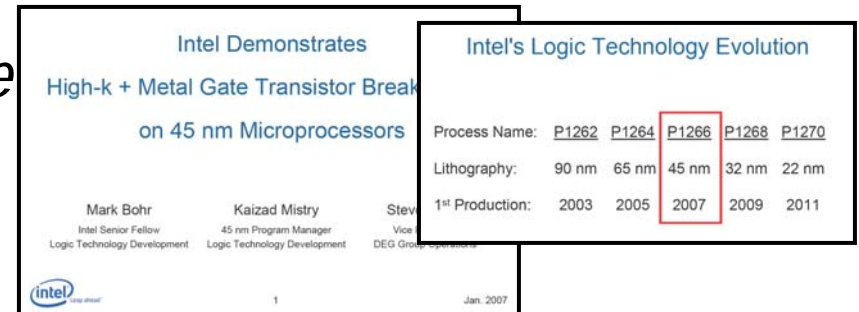
*125 nm & 62 nm nodes  
 $\rightarrow \sim \text{THz devices}$*



*IBM IEDM '06: 65 nm SOI CMOS  $\rightarrow 450 \text{ GHz } f_{max}, \sim 1 \text{ V operation}$*

*Intel Jan '07: 45 nm / high-K / metal gate*

*$\rightarrow$  continued rapid progress*



*What applications for III-V bipolars ?*

*What applications for mm-wave CMOS ?*

# So our focus....

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## *InP Bipolar Transistors*

*what performance can we achieve ?*

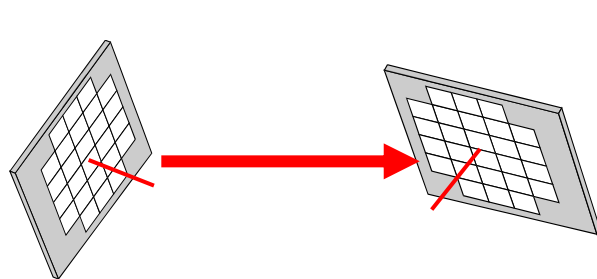
*what are the applications ?*

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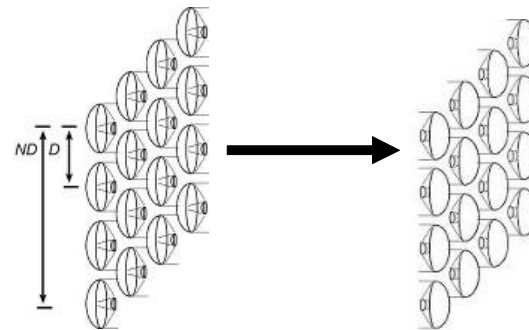
## *65 / 45 / 33 ... nm CMOS*

*vast #s of near-THz transistors*

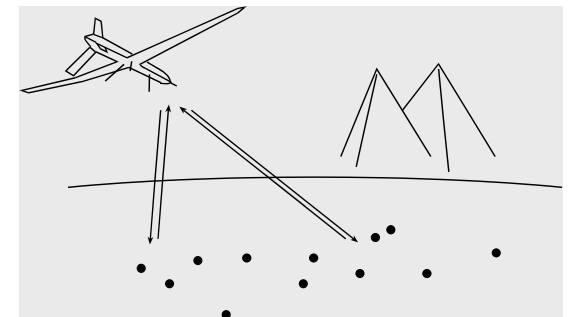
*what **NEW** mm-wave applications will this enable ?*



*massive monolithic mm-wave arrays  
→ 1 Gb/s over ~1 km*



*mm-wave MIMO*



*mm-wave imaging  
sensor networks*

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## *Let's look at InP and CMOS prospects & applications...*

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# *InP Bipolar Transistors*

# InP Bipolar Transistors---what are they for ?

---

## Compared to SiGe:

*~3:1 larger bandwidth at a given feature size*

*~3:1 larger voltage at a given bandwidth*

## Compared to CMOS

*higher bandwidth at 10x the feature size*

*much higher breakdown voltage*

*analog precision*

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## *InP HBT:*

*~ \$10,000 mask cost, ~2-3 month fab cycles*

---

*speed*

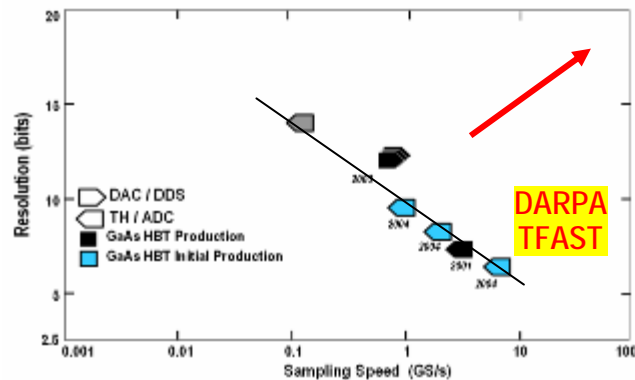
*voltage*

*low volume*

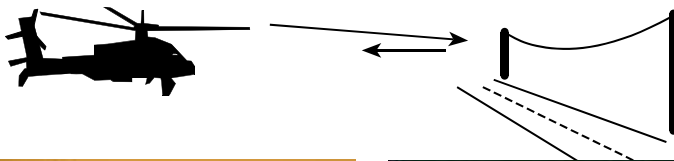
## Applications of THz Transistors

### microwave ADCs and DACs

*more resolution & more bandwidth*



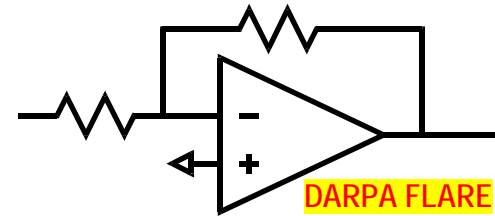
### **340 GHz or 650 GHz imaging systems**



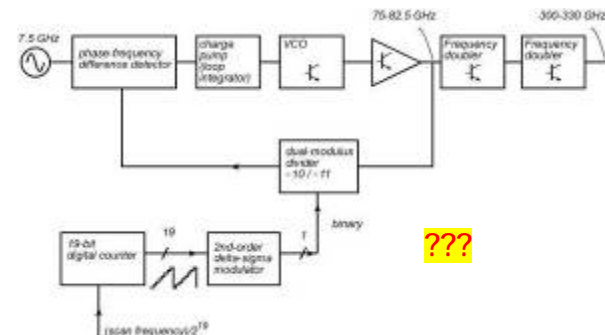
## DARPA SWIFT

### microwave op-amps

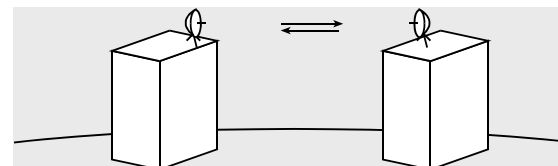
*high IP3 at low DC power at 2-10 GHz*



**single-chip 300-400 GHz spectrometers  
(gas detection)**

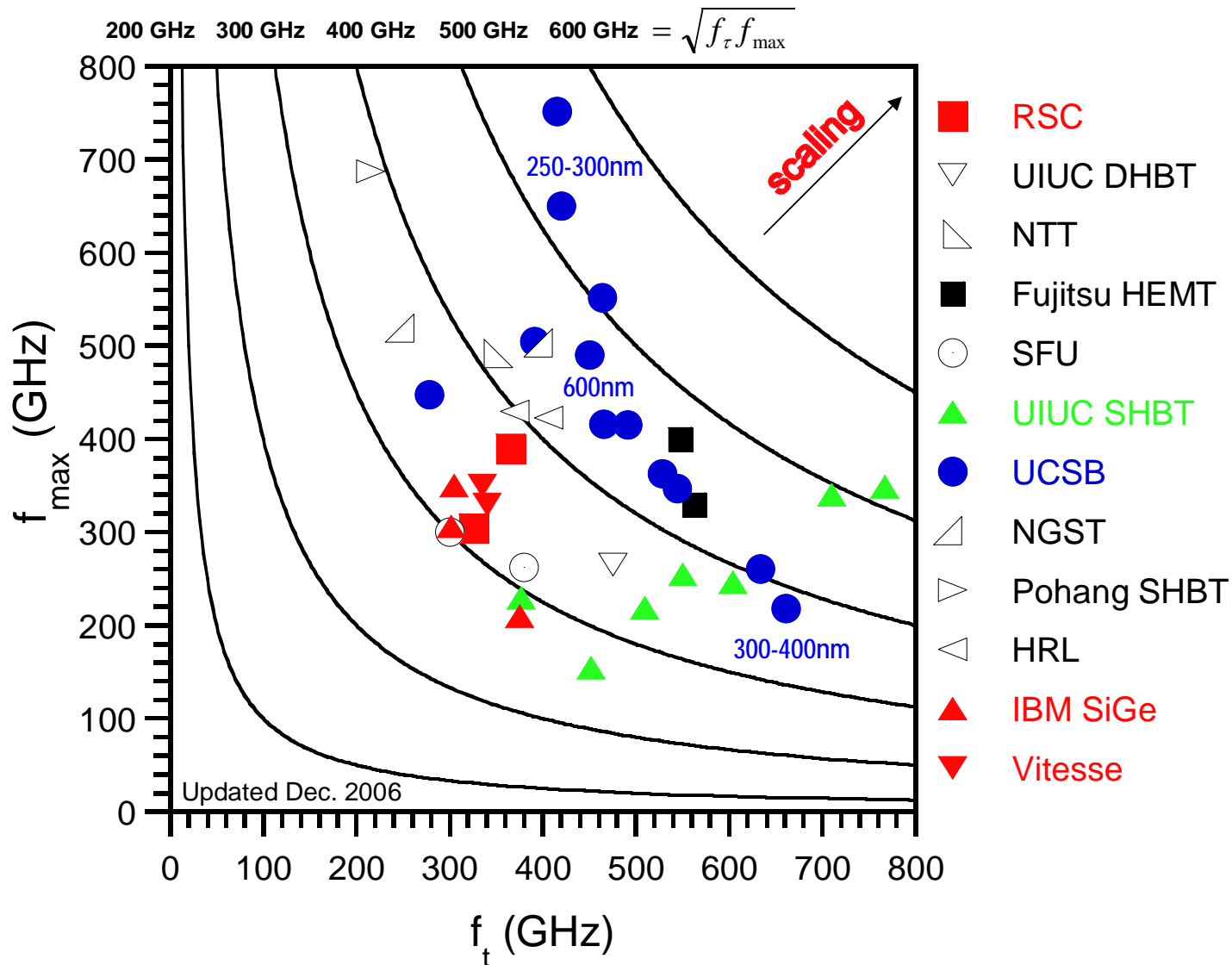


## sub-mm-wave communications





# Present Status: Fast Bipolar Transistors



## popular metrics :

$f_\tau$  or  $f_{\max}$  alone

$(f_\tau + f_{\max}) / 2$

$\sqrt{f_\tau f_{\max}}$

$(1/f_\tau + 1/f_{\max})^{-1}$

## ***much better metrics :***

### power amplifiers :

PAE, associated gain,  
mW/ $\mu\text{m}$

### low noise amplifiers :

$F_{\min}$ , associated gain,

### digital :

$f_{\text{clock}}$ , hence

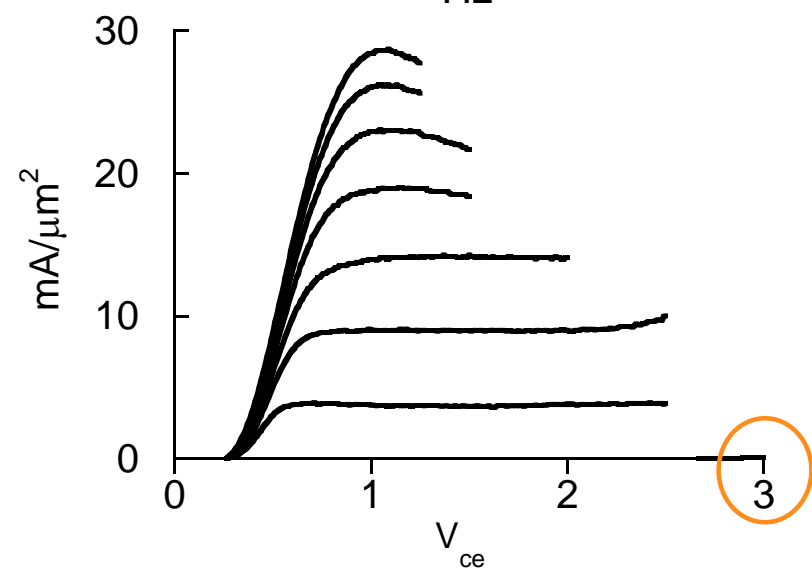
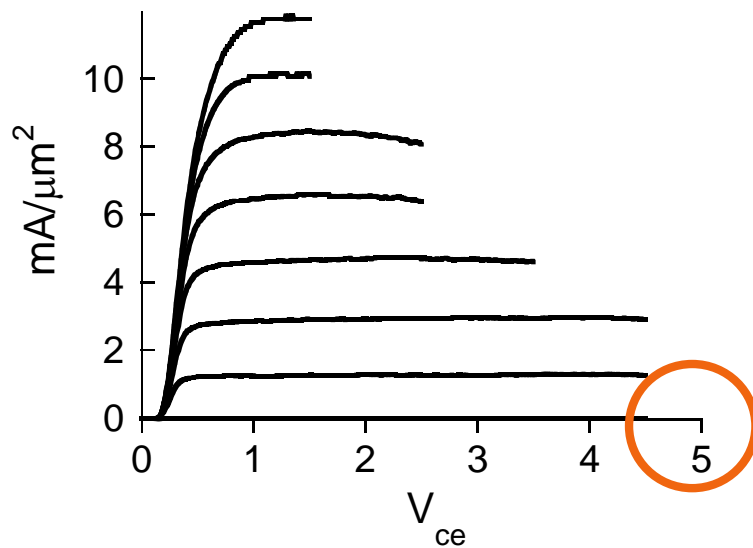
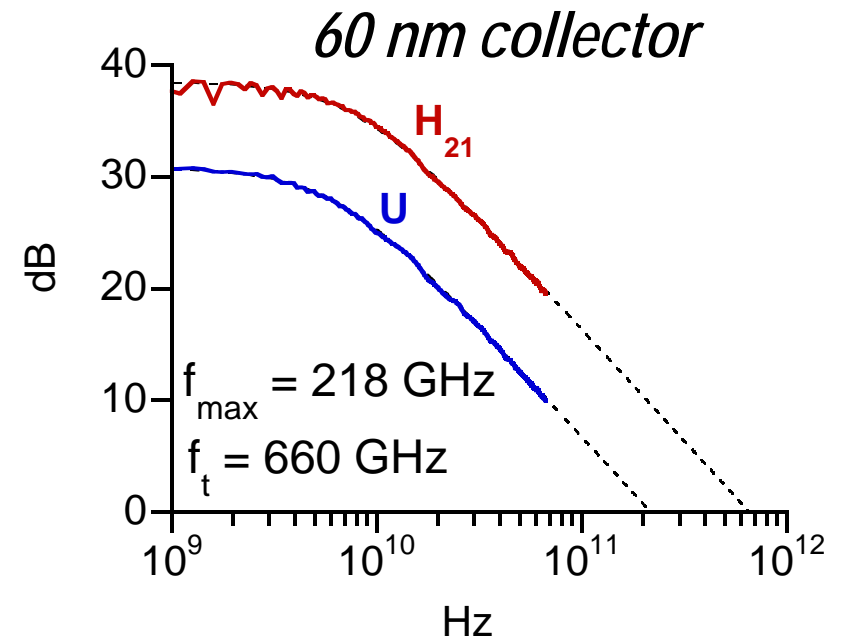
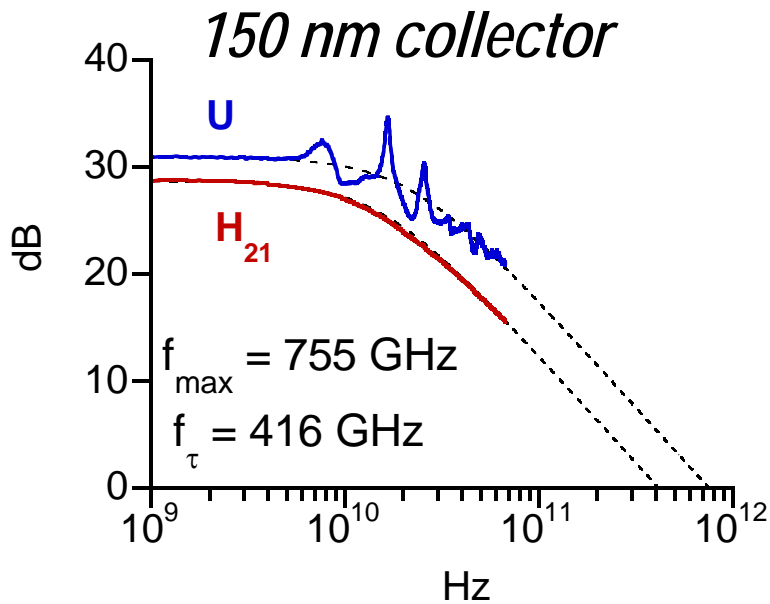
$(C_{cb} \Delta V / I_c)$ ,

$(R_{ex} I_c / \Delta V)$ ,

$(R_{bb} I_c / \Delta V)$ ,

$(\tau_b + \tau_c)$

# UCSB DHBTs: 250 nm Scaling Generation



# 2005: InP DHBTs @ 500 nm Scaling Generation

---

emitter 500 nm width ✓  
16  $\Omega \cdot \mu\text{m}^2$  contact  $\rho$  ✓

base 300 width, ✓  
20  $\Omega \cdot \mu\text{m}^2$  contact  $\rho$  ✓

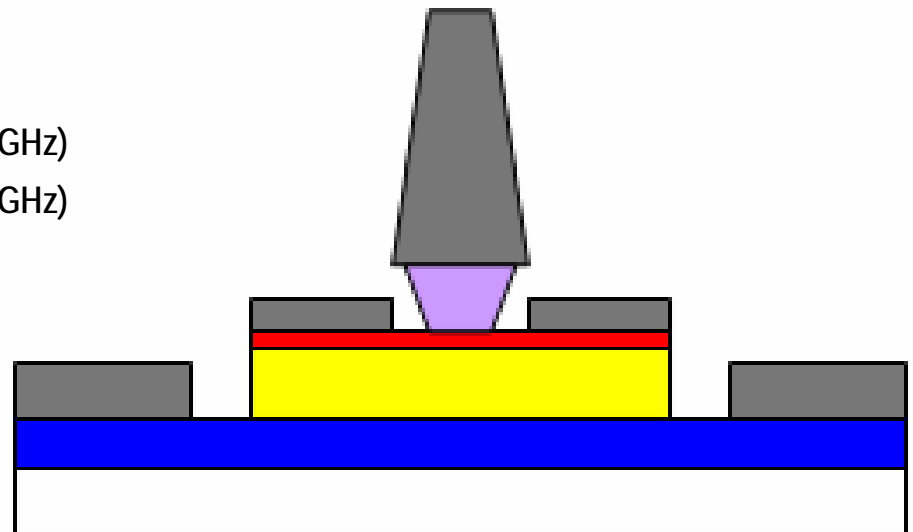
collector 150 nm thick, ✓  
5  $\text{mA}/\mu\text{m}^2$  current density ✓  
5 V, breakdown ✓

$f_\tau$  400 GHz ✓

$f_{\text{max}}$  500 GHz ✓

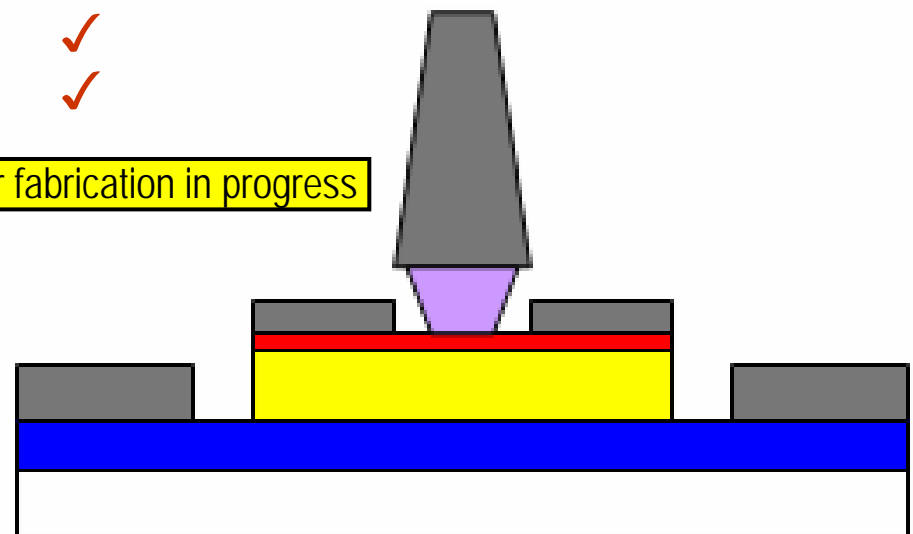
power amplifiers 250 GHz ✓ (178 GHz)

digital clock rate 160 GHz ✓ (150 GHz)  
(static dividers)



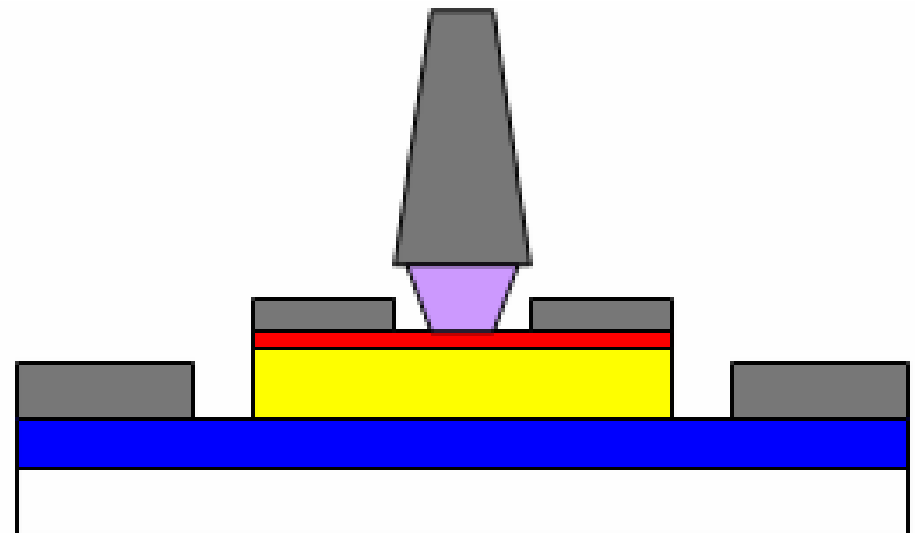
# 2006: 250 nm Scaling Generation, 1.414:1 faster

emitter	500	250 nm width	✓
	16	9 $\Omega \cdot \mu\text{m}^2$ access $\rho$	✓
base	300	150 width,	✓
	20	10 $\Omega \cdot \mu\text{m}^2$ contact $\rho$	✓
collector	150	100 nm thick,	✓
	5	10 mA/ $\mu\text{m}^2$ current density	✓
	5	3.5 V, breakdown	✓
$f_\tau$	400	500 GHz (416 GHz)	✓
$f_{\text{max}}$	500	700 GHz (755 GHz)	✓
power amplifiers	250	350 GHz	Designs and / or fabrication in progress
digital clock rate (static dividers)	160	230 GHz	



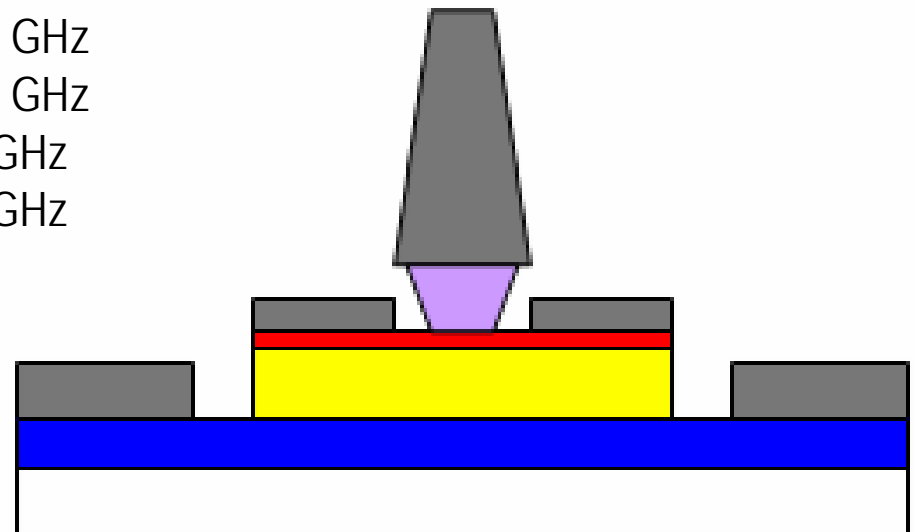
# 2007: 125 nm Scaling Generation → almost-THz HBT

emitter	500	250	125 nm width	✓
	16	9	$4 \Omega \cdot \mu\text{m}^2$ access $\rho$	✓
base	300	150	75 width,	✓
	20	10	$5 \Omega \cdot \mu\text{m}^2$ contact $\rho$	✓
collector	150	100	75 nm thick,	✓
	5	10	$20 \text{ mA}/\mu\text{m}^2$ current density	✓
	5	3.5	3 V, breakdown	✓
$f_\tau$	400	500	700 GHz	
$f_{\text{max}}$	500	700	1000 GHz	
power amplifiers	250	350	500 GHz	
digital clock rate (static dividers)	160	230	330 GHz	



# 2008-9: 65 nm Scaling Generation→beyond 1-THz HBT

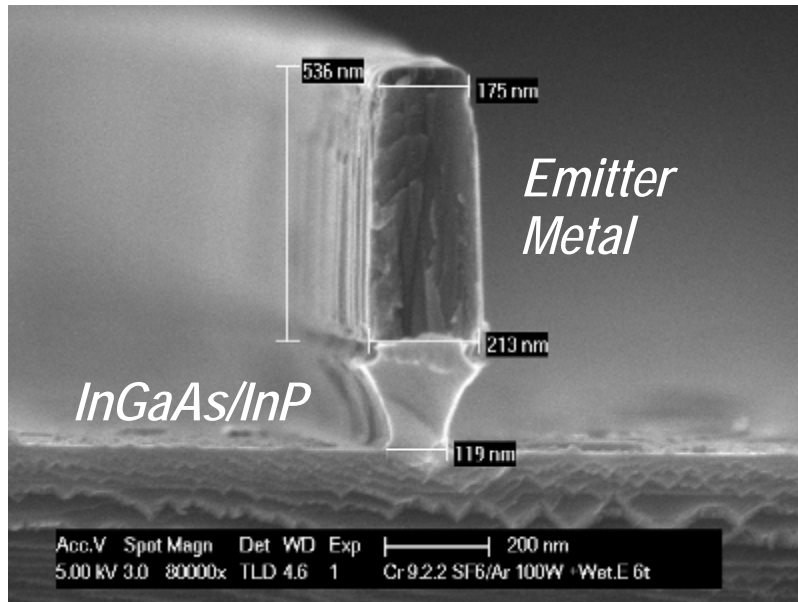
emitter	500 16	250 9	125 4	63 nm width 2.5 $\Omega \cdot \mu\text{m}^2$ access $\rho$ ✓
base	300 20	150 10	75 5	70 nm width, 5 $\Omega \cdot \mu\text{m}^2$ contact $\rho$ ✓
collector	150 5 5	100 10 3.5	75 20 3	53 nm thick, 35 mA/ $\mu\text{m}^2$ current density 2.5 V, breakdown
$f_\tau$	400	500	700	1000 GHz
$f_{\text{max}}$	500	700	1000	1500 GHz
power amplifiers	250	350	500	750 GHz
digital clock rate (static dividers)	160	230	330	450 GHz



# Our first 125 nm DHBTs should come soon:

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*125 nm emitter process  
is ready*



*emitter contact resistivity  
 $\sim 0.7 \Omega \cdot \mu\text{m}^2$*

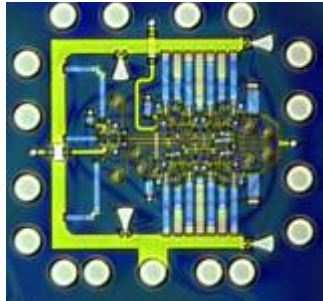
*base contact resistivity  
 $\sim 3\text{-}5 \Omega \cdot \mu\text{m}^2$*

*target performance  $\sim 700\text{-}900$  GHz simultaneous  $f_t$  &  $f_{max}$ ,  
3-4 V breakdown*

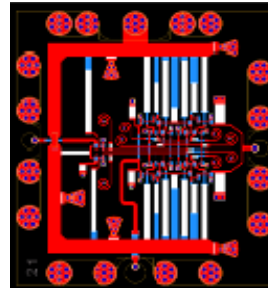
*fabrication runs winter / spring 2007*

# IC designs: Past and Pending

*150 GHz digital latches  
in 500 nm DHBT*

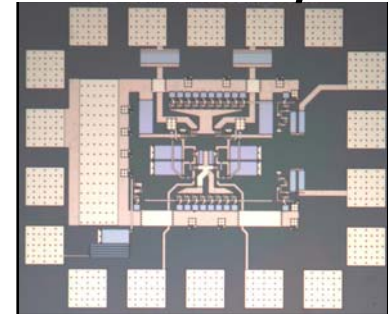


*200 GHz latch designs  
in 250 nm DHBT*



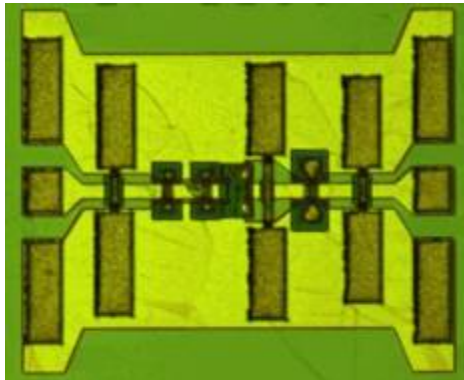
*...fabrication on hold...*

*60 GHz gain-  
bandwidth op-amps*

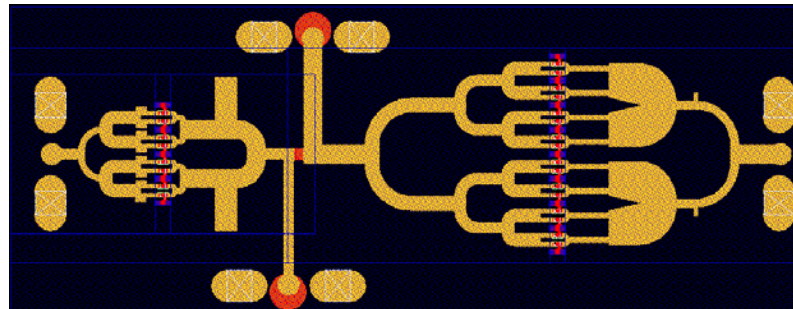


*target:  $OIP3/P_{dc} > 60:1$*

*175 GHz amplifiers  
in 500 nm DHBT*



*340 GHz amplifier designs  
in 250 nm DHBT*



***The proof of a fast transistor is a fast circuit***



# THz CMOS is coming soon

*IBM IEDM '06: 65 nm SOI CMOS  $\rightarrow$  450 GHz  $f_{max}$*

*Intel Jan '07: 45 nm / high-K / metal gate*

Intel's Logic Technology Evolution					
Process Name:	P1262	P1264	P1266	P1268	P1270
Lithography:	90 nm	65 nm	45 nm	32 nm	22 nm
1 <sup>st</sup> Production:	2003	2005	2007	2009	2011

Intel Demonstrates High-k + Metal Gate Transistor Breakthrough on 45 nm Microprocessors		
Mark Bohr Intel Senior Fellow Logic Technology Development	Kaizad Mistry 45 nm Program Manager Logic Technology Development	DEG Group Operations

1 Jan. 2007

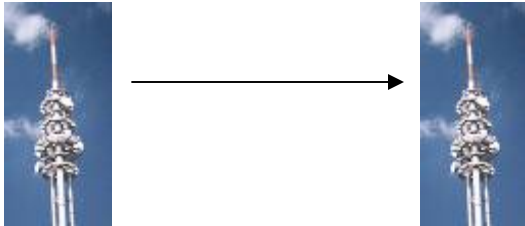
*45 / 33 / 22... nm CMOS*

*vast #s of near-THz transistors*

*what NEW mm-wave applications will this enable ?*

*What could you do with a vast # of high-frequency transistors ?*

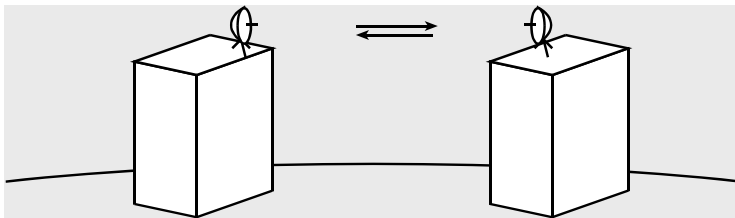
# mm-wave array ICs for Gb/s mobile communications



*mm-wave Bands → Lots of bandwidth*

$$\left( \frac{P_{received}}{P_{transmitted}} \right) = \left( \frac{1}{16\pi^2} \right) \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}$$

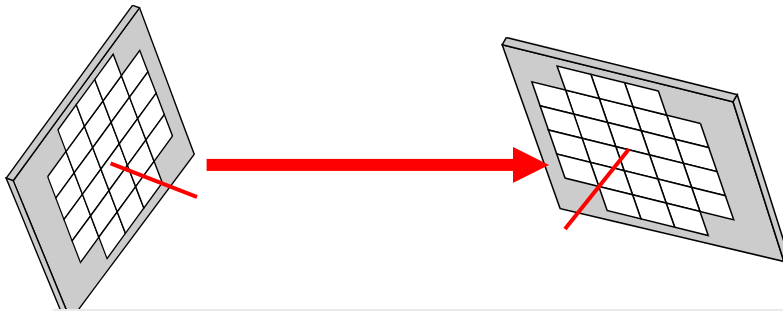
*short wavelength → weak signal → short range*



*highly directional antenna → strong signal → long range*

$$\left( \frac{P_{received}}{P_{transmitted}} \right) = \left( \frac{D_t D_r}{16\pi^2} \right) \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}$$

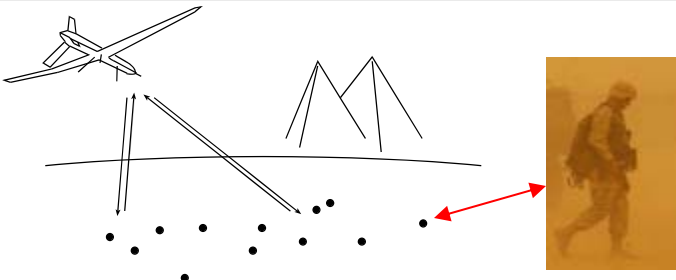
*narrow beam → must be aimed → no good for mobile*



*monolithic beam steering arrays → strong signal, steerable*

$$\frac{P_{received}}{P_{transmit}} = \frac{N_{receive} N_{transmit}}{16} \frac{\lambda^2}{R^2} e^{-\alpha R}$$

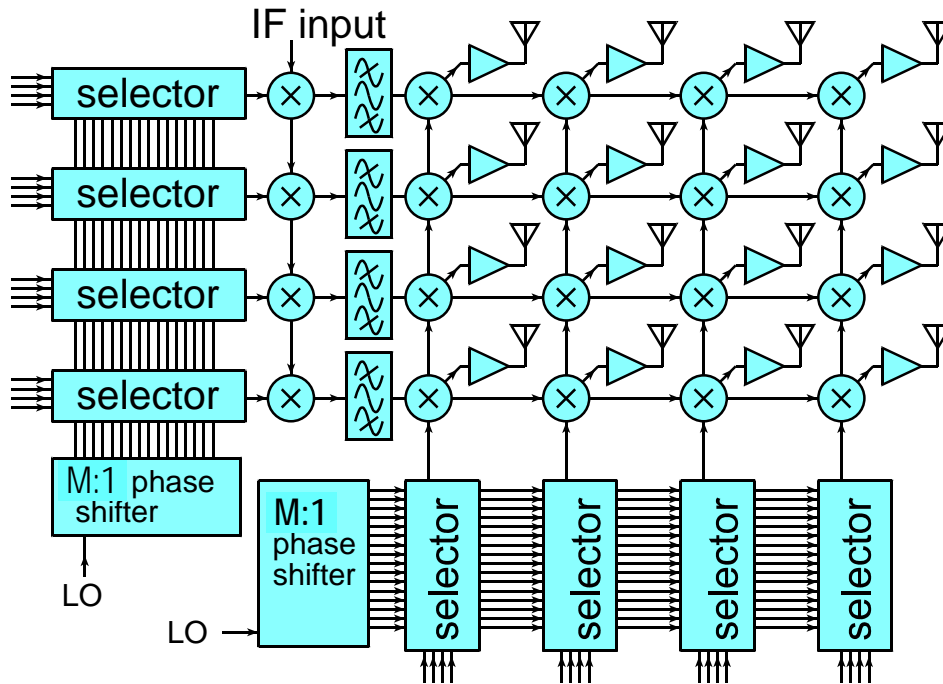
*32 x 32 array → 60-90 dB increased SNR → vastly increased range*



*→ multi-Gigabit  
mobile communications*

# Compact, Massive Monolithic mm-Wave Phased Arrays

*IC architectures scalable to large array sizes*



*Row-Column Architecture---*

*1000-element array requires only 60 phase shifters*

*Mixed-signal IC design*

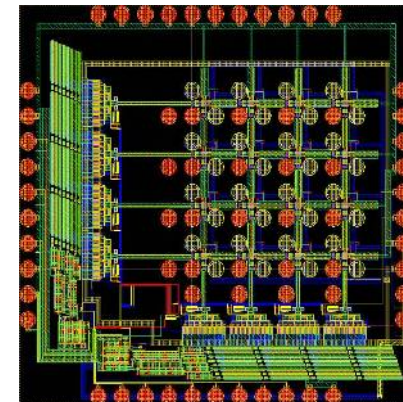
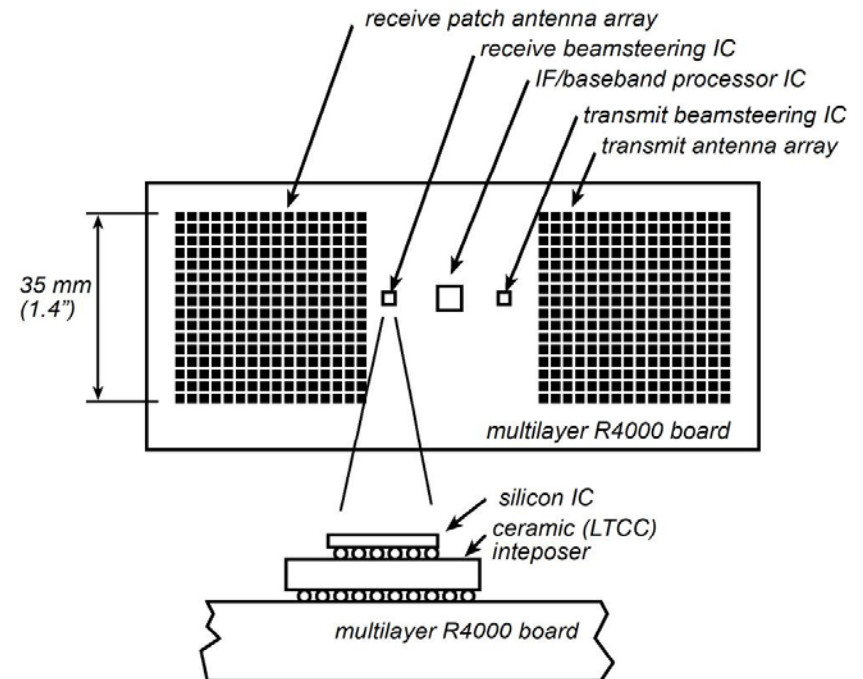
*minimal inductive tuning → robust & compact*

*digital LO phase control → robust & compact*

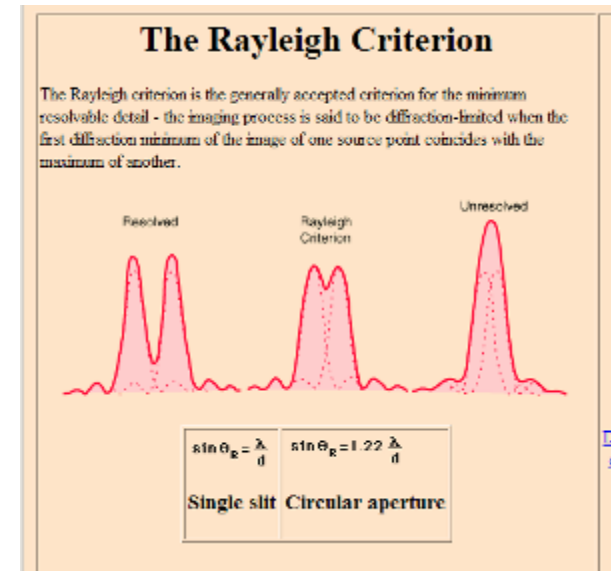
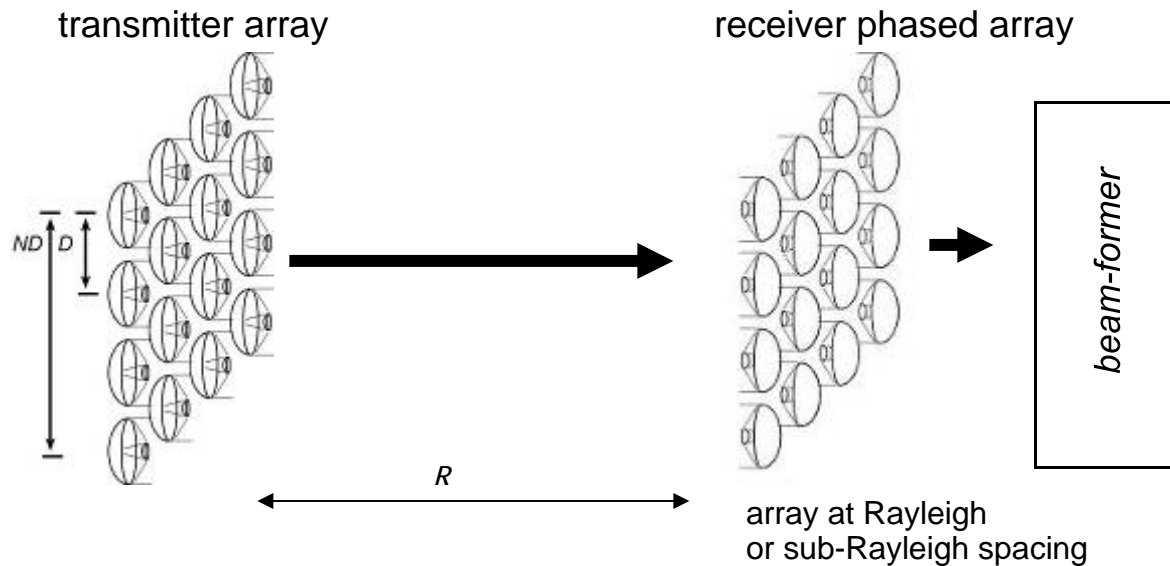
*minimal RF signal propagation → robust*

**"Digital ICs scale, Analog ICs don't"**

*compact circuit-board-based packaging and antennas*



# mm-wave MIMO → wireless at 160 Gb/s rates



**16 wireless communication links, each channel carrying 4QPSK @ 10 Gb/s**  
**Transmitter is  $N \times N$  elements ( $N=4$ ), each transmitting independently**  
**Receiver is  $N \times N$  phased array, with beamformer imaging on the  $N^2$  transmitters**  
**If element spacings meet Rayleigh criterion, then channels do not interfere**

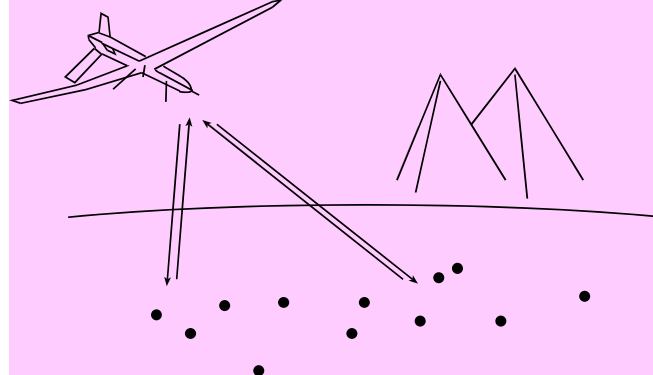
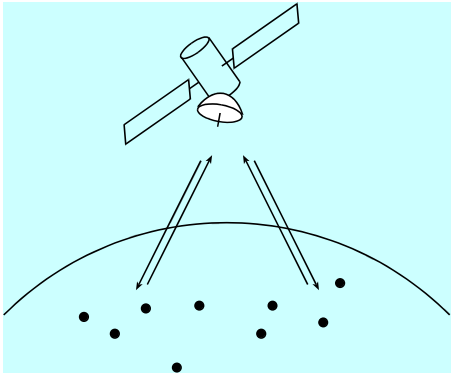
**Feasible range exceeds one mile, even in foul weather**

Spatial angular separation of adjacent transmitters:  $\delta\theta_t = D / R$ ;

Receive array angular resolution:  $\delta\theta_r = \lambda / ND$ ; to resolve adjacent channels,  $\delta\theta_r \leq \delta\theta_t \Rightarrow ND = \sqrt{\lambda NR}$

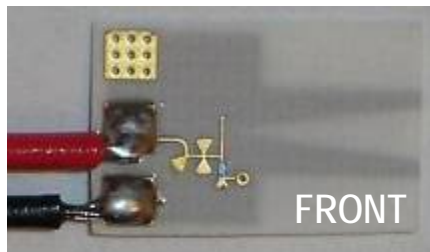
# mm-wave CMOS → Imaging/Radar Sensor Networks

Data collection aircraft : *phased array transmitter / receiver*

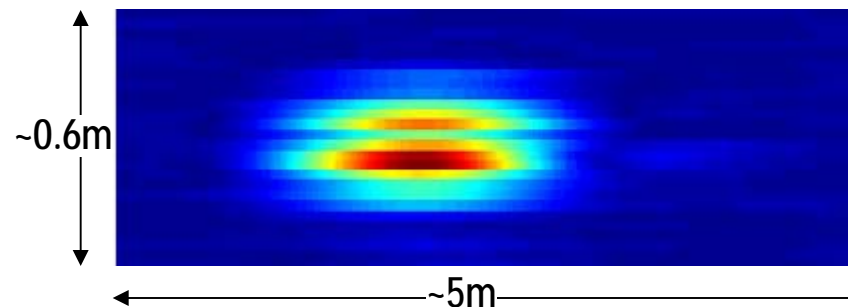
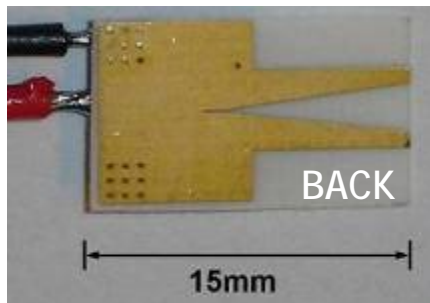


very simple sensors , mm-wave CMOS:  
*passive or active transponders;  
data modulation.  
Range = 10's of km at kb/s rates*

Sensor= Antenna + Modulator



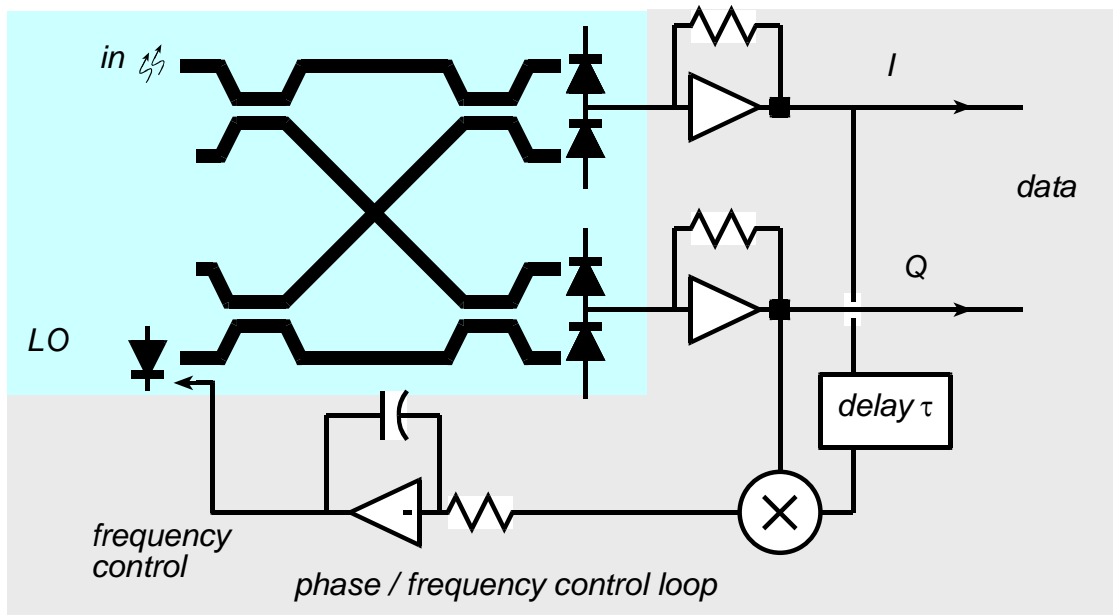
60GHz beacon  
Modulated beacon



*resolving two  
nearby sensors*

*--data is  
also recovered*

# Compact Phase/Frequency-Locked Optical PLLs



*Coherent Optical Receivers*

*Optical Frequency Synthesis*

*Convergence of bandwidths:*

*IC bandwidths > 100 GHz*

*F-P laser frequency (wavelength) precision ~1000 GHz*

*O/E PLL with phase / frequency detection:*

*~200 GHz pull-in range, without scanning*

*→ direct electrical/optical phase-locking*

*...even for inexpensive F-P lasers*

*Compact coherent receivers: QPSK modulation, greatly simplified (DFE/FFE) dispersion compensation*

*Broad tolerance to LO laser phase noise*